What is claimed is:

1. A logic cluster in logic block of a field programmable gate array, comprising:

a first look-up table (LUT) having a plurality of inputs and a single output;

a second LUT having a plurality of inputs and a single output;

a D-type flip-flop having an input and an output;

a first n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a first signal and said source connected to said output of said first LUT;

a second n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a second signal, said source connected to said output of said second LUT and said drain connected to said drain of said first n-channel MOS pass transistor to form a node connected to said input of said D-type flip-flop;

a third n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said first signal and said source connected to said output of said first LUT;

a fourth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said second signal and said source connected to said output of said second LUT;

a fifth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to said first signal and said source connected to said drain of said third n-channel MOS pass transistor;

a sixth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to said second signal, said source connected to said drain of said fourth n-channel MOS pass transistor and said drain connected to said drain of said fifth n-channel MOS pass transistor to form a node connected to said output of said D-type flip-flop;

a first inverter having an input and an output, said input connected to said drain of said third n-channel MOS pass transistor;

a second inverter having an input and an output, said input connected to said drain of said fifth n-channel MOS pass transistor;

a seventh n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a third signal and said source connected to said output of said first inverter;

an eighth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said third signal, said source connected to said output of said second inverter and said drain connected to said drain of said seventh n-channel MOS pass transistor to form a node as a first output of said logic cluster;

a ninth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a fourth signal and said source connected to said output of said second inverter; and

a tenth n-channel MOS pass transistor having a gate, a source and a drain, said gate coupled to a complement of said fourth signal, said source connected to said output of said first inverter and said drain connected to said drain of said ninth n-channel MOS pass transistor to form a node as a second output of said logic cluster.